according to the present invention. Unless such changes and modifications obtained made by those skilled in the art through the application of various modifications to the exemplary embodiments or through a combination of the features of the exemplary embodiments depart from the scope of the present invention, they should be construed as being included therein.

INDUSTRIAL APPLICABILITY

[0170] The method of manufacturing a non-volatile semiconductor memory device according to the present invention simplifies a process of manufacturing an element by forming a shared electrode by performing the plasma nitriding process on an upper surface of the variable resistance layer, the shared electrode serving as both an upper electrode of a variable resistance element and a lower electrode of a non-ohmic element. Moreover, the method according to the present invention can reduce variations in characteristics of the non-ohmic elements, stabilize the resistance to pressure of the non-ohmic elements, and implement miniaturization of the non-volatile memory element. Thus, the present method is useful in various electronics fields requiring memory devices that are compact in size and stable in characteristics.

REFERENCE SIGNS LIST

[0171] **5** Word line decoder
[0172] **6** Bit line decoder
[0173] **7** Read circuit
[0174] **10**, **40**, **70**, **1000** Non-volatile semiconductor memory device
[0175] **11** Substrate
[0176] **12** Active element
[0177] **12***a* Source region
[0178] **12***b* Drain region
[0179] **12***c* Gate insulating film
[0180] **12***d* Gate electrode
[0181] **13**, **14**, **16**, **30**, **31**, **47**, **48**, **52**, **102**, **109** Interlayer insulating layer
[0182] **15**, **71**, **101** Lower electrode line
[0183] **15***a*, **201** First electrode
[0184] **17**, **41**, **53**, **75**, **103**, **206**, **1260** Variable resistance element
[0185] **18**, **42**, **54**, **76**, **104**, **202**, **212**, **1230** Variable resistance layer
[0186] **19**, **43**, **55**, **79**, **105**, **203** Shared electrode
[0187] **20**, **33**, **44**, **56**, **78**, **106**, **207** Non-ohmic element
[0188] **21**, **34**, **45**, **57**, **80**, **107**, **204** Semiconductor layer (semiconductor layer or insulating layer)
[0189] **22**, **35**, **46**, **58**, **81**, **108**, **1240** Upper electrode (second electrode)
[0190] **23**, **60** Insulation protection layer (interlayer insulating layer)
[0191] **24**, **25**, **28**, **50**, **51** Buried conductor
[0192] **26** Line
[0193] **27**, **27***a*, **49**, **49***a*, **59**, **110** Upper layer line
[0194] **29** Memory cell hole
[0195] **30***a* First insulating layer
[0196] **30***b* Second insulating layer
[0197] **32** Trench
[0198] **72** Lower line
[0199] **73**, **73***a*, **82** Connection electrode
[0200] **181** Resistance film layer
[0201] **205** Second electrode
[0202] **341** Semiconductor film layer (semiconductor film layer or insulator film layer)
[0203] **351** Electrode film layer

1-9. (canceled)

10. A method of manufacturing a non-volatile semiconductor memory element including a variable resistance element and a non-ohmic element connected in series with the variable resistance element,
the variable resistance element including (i) a first electrode, (ii) a variable resistance layer formed on the first electrode, and (iii) a shared electrode formed in an upper part of the variable resistance layer,
the non-ohmic element including (i) the shared electrode, (ii) one of a semiconductor layer and an insulator layer formed on the shared electrode, and (iii) a second electrode formed on the one of the semiconductor layer and the insulator layer, and
the method comprising:
forming the first electrode on a substrate;
forming the variable resistance layer on the first electrode, the variable resistance layer comprising an oxide of a transition metal;
forming the shared electrode having a front surface comprising a nitride of the transition metal, by replacing oxygen atoms in a front surface part of the variable resistance layer with nitrogen atoms by nitriding a front surface of the variable resistance layer;
forming the one of the semiconductor layer and the insulator layer on the shared electrode; and
forming the second electrode on the one of the semiconductor layer and the insulator layer,
wherein the front surface of the shared electrode comprises the nitride of the transition metal including the transition metal and nitrogen, so that a Schottky barrier is formed in an interfacial surface between the shared electrode and the semiconductor or insulator layer.

11. The method of manufacturing the non-volatile semiconductor memory element according to claim **10**,
wherein the oxide of the transition metal is one of a tantalum oxide and a hafnium oxide, and
a front surface of the one of the tantalum oxide and the hafnium oxide is nitrided so as to form the shared electrode having a front surface comprising a corresponding one of a tantalum nitride and a hafnium nitride.

12. The method of manufacturing the non-volatile semiconductor memory element according to claim **10**,
wherein the variable resistance layer includes:
a first transition metal oxide layer formed on the first electrode; and
a second transition metal oxide layer that is formed on the first transition metal oxide layer and has a lower oxygen content atomic percentage than the first transition metal oxide layer.

13. A method of manufacturing a cross point non-volatile semiconductor memory device including a plurality of non-volatile semiconductor memory elements arranged in an array, each of the non-volatile semiconductor memory elements having a variable resistance element and a non-ohmic element connected in series with the variable resistance element,
the variable resistance element including (i) a lower electrode line formed to be shared by, among the non-volatile semiconductor memory elements arranged in the array, non-volatile semiconductor memory elements